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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Tian et al.

Serial No.: 10/677,414

Filed: October 2, 2003

Assignee: Intel Corporation

For: Methods And Apparatus For Reducing Memory Latency In A Software Application

Group Art Unit: 2121

Examiner: Unknown

I hereby certify that this paper is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this date:

DATED: January 15, 2004

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Registration No. 44,006
Attorney for Applicant(s)

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The patents and/or publications listed on the enclosed PTO Form-1449 are submitted pursuant to 37 CFR §§ 1.56, 1.97, and 1.98. Copies of the patents or publications are enclosed.

TIME OF FILING

This information disclosure statement is being filed to the best of the undersigned's knowledge, before the mailing date of a first Office action on the merits. In accordance with 37 CFR §1.97(b), no certification or fee is required.

METHOD OF PAYMENT

☒ No fee is required.

The Commissioner is authorized to charge any fee deficiency required by this paper, or credit any overpayment, to Deposit Account No. 50-2455. A copy of this paper is enclosed.

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Respectfully submitted,

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Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. 20002/17225	Serial No. 10/677,414
INFORMATION DISCLOSURE STATEMENT (*Use several sheets if necessary*)		Applicant TIAN et al.	
		Filing Date **10/02/03**	Group Art Unit 2121

		S. Liao, P. Wang, H. Wang, G. Hoflehner, D. Lavery, J. Shen. "Post-Pass Binary Adapation For Software-Based Speculative Precomputation." Proceedings of the ACM SIGPLAN 2002 Conference On Programming Language Design And Implementation. 2002.
		H. Wang, P. Wange, R. Weldon, S. Ettinger, H. Saito, M. Girkar, S. Liao, J. Shen. Speculative Precomputation: Exploring the Use of Multithreading for Latency. In *Intel Techonology Journal* Q1, 2002. Vol. 6 Issue 1.
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EXAMINER	DATE CONSIDERED
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not cinsidered. Include copy of this form with next communication to applicant.	

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U.S. PATENT DOCUMENTS							
*EXAMINER INITIALS		DOCUMENT NUMBER	ISSUE DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS								
*Examiner Initials		Document Number	Publication Date	Country	Class	Subclass	Translation Yes	No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)		
	✓	M. Annavaram, J. Patel, E. Davidson. Data Prefetching by Dependence Graph Precomputation. In *28th International Symposium on Computer Architecture*, Goteborg, Sweden, July 2001.
	✓	M. Carlisle. Olden: Parallelizing Programs with Dynamic Data Structures on Distributed-Memory Machines, *Ph.D. Thesis*, Princeton University Department of Computer Science, June 1996.
	✓	R. Chappell, J. Stark, S. Kime, S. Reinhardt, and Y. Patt. Simultaneous Subordinate Microthreading (SSMT). In *26th International Symposium on Computer Architecture*, May 1999.
	✓	J. Collins, H. Wang, D. Tullsen, C. Hughes, Y. Lee, D. Lavery, J. Shen. Speculative Precomputation: Long-range Prefetching of Delingquent Loads. In *28th International Symposium on Computer Architecture*, Goteborg, Sweden, July 2001.
	✓	Intel Corporation. "Intel delivers Hyper-Threading Technology with Pentium 4 Processor 3 Ghz milestone." http://www.intel.com/pressroom /archive/release/20021114comp.htm. As printed on Jan. 12, 2003.
	✓	D. Kim and D. Yeung. Design and Evaluation of Compiler Algorithms for Pre-Exectution. In *ASPLOS-X Conference*, pp. 159-170, October 2002.

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